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5/11/06.

IN THE SPECIFICATION:

Paragraph beginning at line 2 of page 8 has been amended as follows:

Embodiments of the present invention will be described below with reference to the accompanying drawings. Fig. 1 is a schematic sectional view of an N-channel vertical MOS transistor according to the present invention. A semiconductor substrate shown in Fig. 1 is prepared by forming, through epitaxial growth, on a heavily doped substrate 1 of a first conductivity type which serves as a drain region, a first conductivity type layer 2 doped with an impurity that is used to dope the substrate 1 in a concentration lower than that of the substrate 1. A surface of the thus prepared semiconductor substrate is subjected to impurity implantation and subsequent high temperature heat treatment at 1,000°C or more to form a diffusion region 3 of a second conductivity type, which serves, as a body region. The other portions of the surface of the substrate constitute a high concentration impurity region 7 of the first conductivity type which serves as a source region and a heavily doped body contact region 8 of the second conductivity type which fixes an electric potential of the body region by ohmic contact. The regions 7 and 8 are turned conductive by the same metal